ABSTRACT

A memory cell array is included which is constituted by arranging the plurality of nonvolatile memory cells in a row direction and column direction respectively and arranging the plurality of word lines (WL) and the plurality of bit lines (BL) in the row direction and the column direction respectively in order to select a predetermined memory cell or a memory cell group out of the arranged nonvolatile memory cells, in which the memory cells are respectively constituted by connecting one end of a variable resistive element for storing information in accordance with a change of electrical resistances with the source of a selection transistor while in the memory cell array, the drain of the selection transistor is connected with a common bit line (BL) along the column direction, the other end of the variable resistive element is connected with a source line (SL), and the gate of the selection transistor is connected with the common word line (WL) along the row direction. According to the above memory cell configuration, it is possible to provide a nonvolatile semiconductor memory device capable of reducing voltage stresses applied to the variable resistive element of an unselected memory cell at the time of the reading and programming operations and securing a higher-reliability data holding characteristic.

Reference Drawing: Fig. 2